Exhibit D

[redacted]

UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC., Plaintiff, vs. SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC., Defendants.	)	Case No. 2:22-cv-293-JRG JURY TRIAL DEMANDED LEAD CASE
NETLIST, INC., Plaintiff, vs. MICRON TECHNOLOGY, INC.; MICRON SEMICONDUCTOR PRODUCTS, INC.; MICRON TECHNOLOGY TEXAS LLC, Defendants.	)	Case No. 2:22-cv-294-JRG JURY TRIAL DEMANDED

THIRD AMENDED COMPLAINT AGAINST SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., AND SAMSUNG SEMICONDUCTOR, INC.

1. Plaintiff Netlist, Inc. (“Netlist”), by its undersigned counsel, for its Second Amended Complaint against defendants Samsung Electronics Co., Ltd. (“SEC”), Samsung Electronics America, Inc. (“SEA”), and Samsung Semiconductor, Inc. (“SSI”) (collectively, “Samsung” or “Defendants”), states as follows, with knowledge as to its own acts, and on information and belief as to the acts of others:

2. This action involves Netlist's U.S. Patent Nos. 7,619,912 (the "'912 patent," Exhibit 1), 11,093,417 (the "'417 patent," Exhibit 2), 9,858,215 (the "'215 patent," Exhibit 3), and 10,268,608 (the "'608 patent") (the "Patents-in-Suit").

I. THE PARTIES

3. Plaintiff Netlist is a corporation organized and existing under the laws of the State of Delaware, having a principal place of business at 111 Academy Drive, Suite 100, Irvine, CA 92617.

4. On information and belief, SEC is a corporation organized and existing under the laws of the Republic of Korea, with its principal place of business at 129 Samsung-ro, Yeongtong-gu, Suwon, Gyeonggi, 16677, Republic of Korea. On information and belief, SEC is the worldwide parent corporation for SEA and SSI, and is responsible for the infringing activities identified in this Second Amended Complaint. On information and belief, SEC's Device Solutions division is involved in the design, manufacture, use, offering for sale and/or sales of certain semiconductor products, including the Accused Instrumentalities as defined below. On information and belief, SEC is also involved in the design, manufacture, and provision of products sold by SEA.

5. On information and belief, SEA is a corporation organized and existing under the laws of the State of New York. On information and belief, SEA, collectively with SEC, operates the Device Solutions division, which is involved in the design, manufacture, use, offering for sale and/or sales of certain semiconductor products, including the Accused Instrumentalities as defined below. Defendant SEA maintains facilities at 6625 Excellence Way, Plano, Texas 75023. SEA may be served with process through its registered agent for service in Texas: CT Corporation System, 1999 Bryan Street, Suite 900, Dallas, Texas 75201-3136. SEA is a wholly owned subsidiary of SEC.

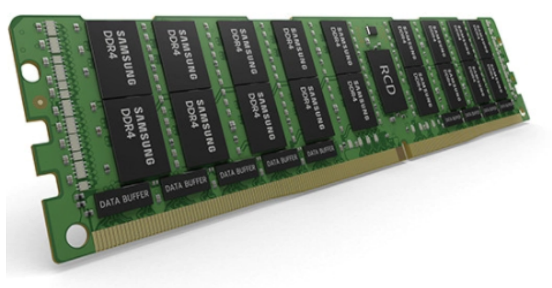
customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Samsung has contributed to, and currently contributes to, Samsung's customers and end-users infringement of the '215 patent through its affirmative acts of selling and offering to sell, in this District and elsewhere in the United States, the accused DDR4 LRDIMM products and other materially similar products that infringe the '215 patent. On information and belief, the accused DDR4 LRDIMM and other materially similar products have no substantial noninfringing use, and constitute a material part of the patented invention. On information and belief, Samsung is aware that the product or process that includes the accused DDR4 LRDIMM products and other materially similar products would be covered by one or more claims of the '215 patent. On information and belief, the use of the product or process that includes the accused DDR4 LRDIMM products infringes at least one claim of the '215 patent.

68. Samsung's infringement of the '215 patent has damaged and will continue to damage Netlist. Samsung has had knowledge of Netlist's technology since as early as 2010. Samsung gained knowledge of predecessor patents to the '215 patent in a 2012 presentation and a 2015 presentation. Samsung also gained knowledge of predecessor patents to the '215 patent in 2016 when, upon Samsung's request, Netlist provided Samsung with a list of its patents and the products they cover. Samsung gained knowledge of the '215 patent no later than August 2, 2021, when Netlist provided Samsung with a list of its patents, including the '215 patent. Samsung's infringement of the '215 patent has been continuous and willful. Samsung continues to commit acts of infringement despite a high likelihood that its actions constitute infringement, and Samsung knew or should have known that its actions constituted an unjustifiably high risk of infringement.

VII. FOURTH CLAIM FOR RELIEF – '608 PATENT

69. Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this Second Amended Complaint as if fully set forth herein.

70. To the extent the preamble is limiting, each of the accused DDR4 LRDIMMs comprise a memory module operable to communicate with a memory controller via a memory bus. As an example, Samsung's website markets and contains datasheets for the accused DDR4 LRDIMMs:



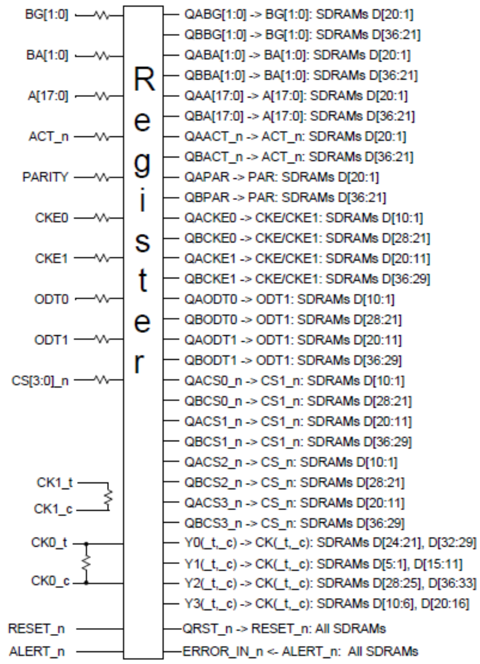
LRDIMM

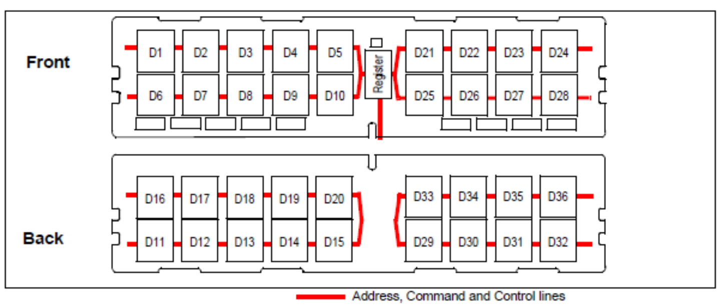
Load Reduced DIMM

- Include a register for enhancing clock, command and control signals
- Enhanced data signal by placing data buffer
- Best solution for achieving high density with high speed
- Supports x4 Organization / up to 4 ranks per DIMM and 3DPC
- Application : Server

(Depiction of an exemplary Samsung DDR4 LRDIMM advertised on its website, *available at* https://semiconductor.samsung.com/dram/module/lrdimm/m386a8k40bm1-crc/ (last accessed August 13, 2022)).

71. The memory bus of each accused LRDIMMs has signal lines that include a set of control/address signal lines and a plurality of sets of data/strobe signal lines.





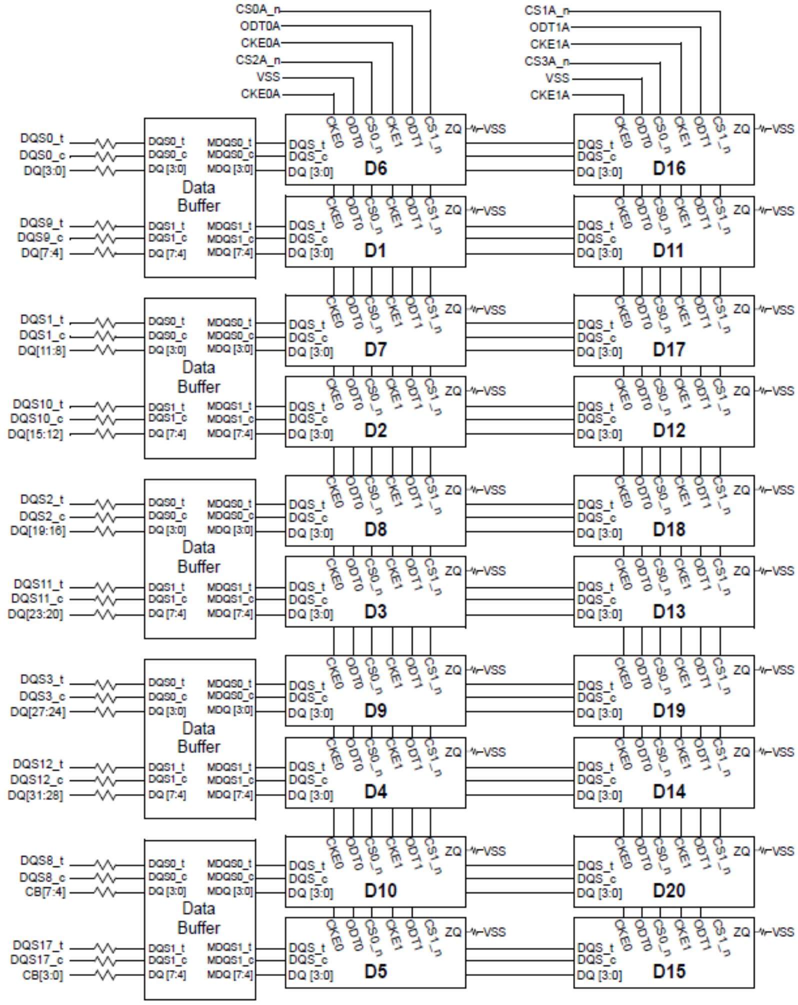
Ex. 6 at 10 (datasheet for M386A8K40BM1-CRC) (showing control/address signal lines).

5. Pin Description

Pin Name	Description	Pin Name	Description
A0–A17[1]	Register address input	SCL	I2C serial bus clock for SPD/TS and register
BA0, BA1	Register bank select input	SDA	I2C serial bus data line for SPD/TS and register
BG0, BG1	Register bank group select input	SA0–SA2	I2C slave address select for SPD/TS and register
RAS_n[2]	Register row address strobe input	PAR	Register parity input
CAS_n[3]	Register column address strobe input	VDD	SDRAM core power supply
WE_n[4]	Register write enable input	VPP	SDRAM activating power supply
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	VREFCA	SDRAM command/address reference supply
CKE0, CKE1	Register clock enable lines input	VSS	Power supply return (ground)
ODT0, ODT1	Register on-die termination control lines input	VDDSPD	Serial SPD/TS positive power supply
ACT_n	Register input for activate input	ALERT_n	Register ALERT_n output
DQ0–DQ63	DIMM memory data bus	RESET_n	Set Register and SDRAMs to a Known State
CB0–CB7	DIMM ECC check bits	EVENT_n	SPD signals a thermal event has occurred
DQS0_t–DQS17_t	Data Buffer data strobes (positive line of differential pair)	VTT	SDRAM I/O termination supply
DQS0_c–DQS17_c	Data Buffer data strobes (negative line of differential pair)	RFU	Reserved for future use
CK0_t, CK1_t	Register clock input (positive line of differential pair)		
CK0_c, CK1_c	Register clocks input (negative line of differential pair)		

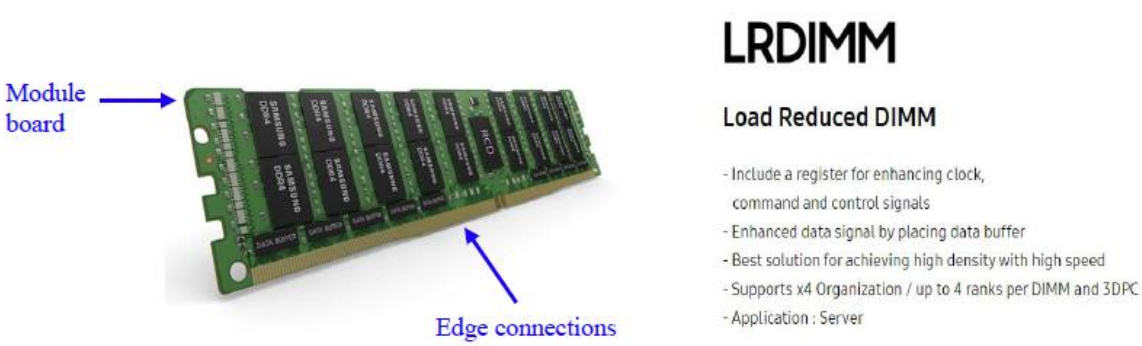
NOTE :
1. Address A17 is only valid for 16 Gb x4 based SDRAMs.
2. RAS_n is a multiplexed function with A16.
3. CAS_n is a multiplexed function with A15.
4. WE_n is a multiplexed function with A14.

Id. at 6.



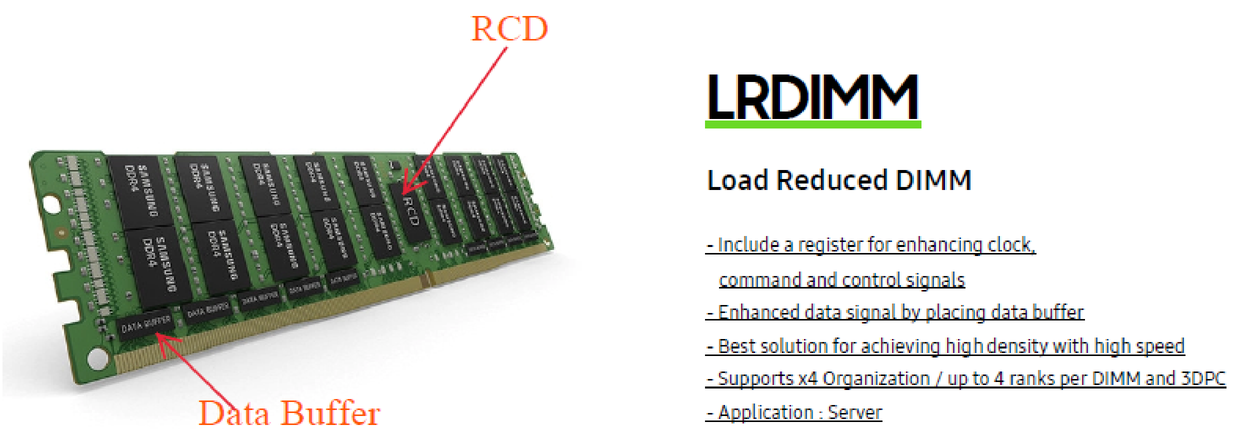
Id. at 11 (datasheet for M386A8K40BM1-CRC (showing the data/strobe signal lines)).

72. The accused DDR4 LRDIMMs further each comprise a module board having edge connections to be coupled to respective signal lines in the memory bus, as illustrated in the examples below.



(Annotated depiction of an exemplary Samsung DDR4 LRDIMM advertised on its website, *available at* https://semiconductor.samsung.com/dram/module/lrdimm/m386a8k40bm1-crc/ (last accessed August 13, 2022)); *see also* Ex. 6 at 42 (datasheet for M386A8K40BM1-CRC).

73. The accused DDR4 LRDIMMs further each comprise a module control device (*e.g.*, a registering clock driver, or "RCD") on the module board configurable to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals. The module control device in each accused DDR4 LRDIMM is also configured to receive a system clock signal and output a module clock signal (*e.g.*, BCK_t/c). For example,

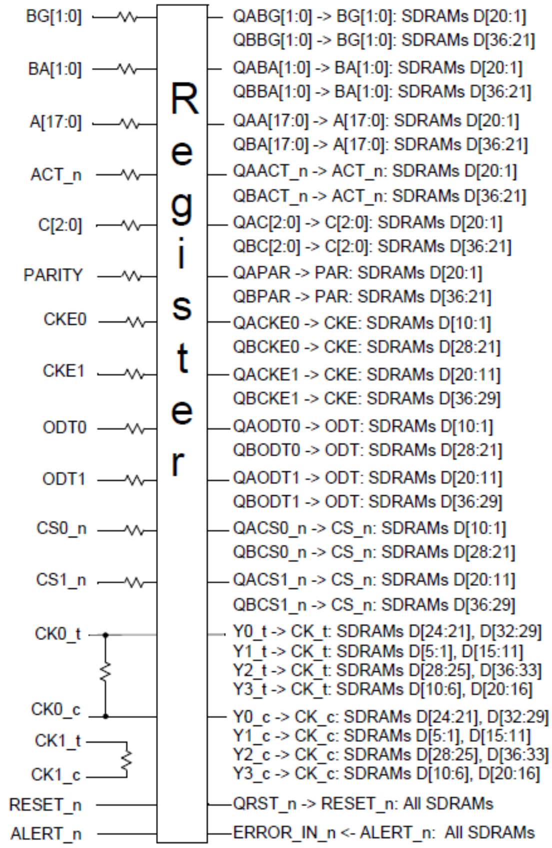


(Annotated depiction of an exemplary Samsung DDR4 LRDIMM advertised on its website, *available at* https://semiconductor.samsung.com/dram/module/lrdimm/m386a8k40bm1-crc/ (last accessed August 13, 2022)).

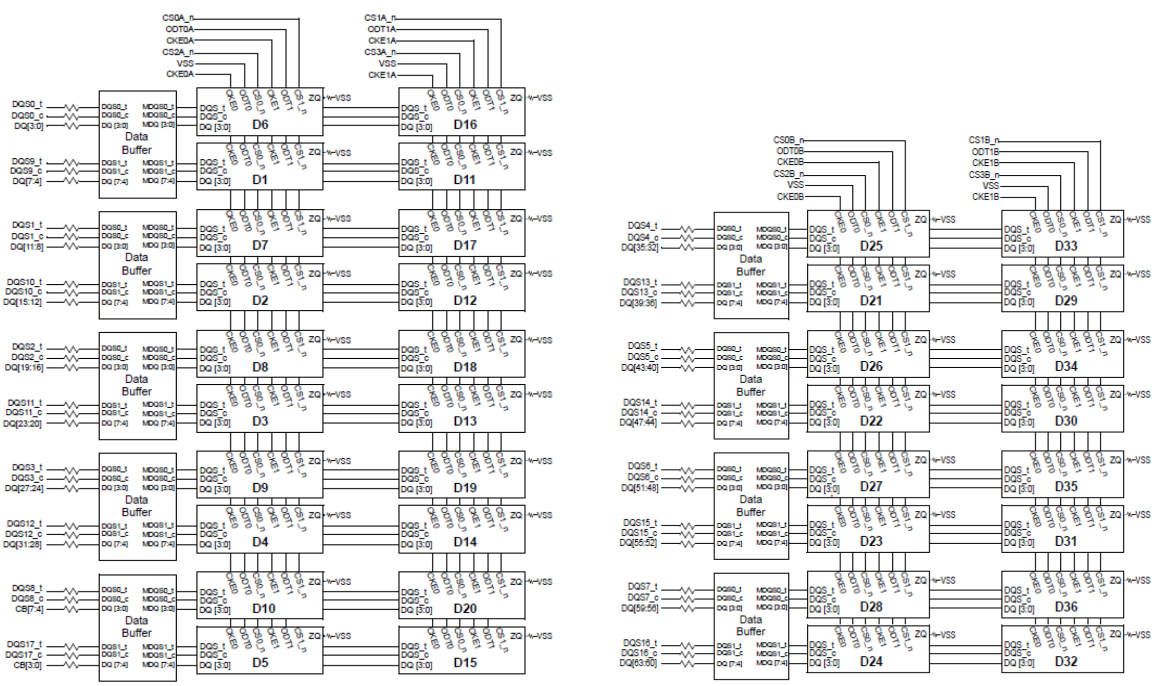
7. Input/Output Functional Description

Symbol	Type	Function
CK0_t, CK0_c CK1_t, CK1_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE0, CKE1	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c, ODT and CKE, are disabled during power-down. Input buffers,excluding CKE, are disabled during Self-Refresh.
CS0_n, CS1_n CS2_n, CS3_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0, C1	Input	Chip ID : Chip ID is only used for 3DS for 2and4 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.
ODT0, ODT1	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/, signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16. CAS_n/A15. WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addresses like A16, A15 and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write and other command defined in command truth table
DM_n/DBI_n	Input/ Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10, A11, A12 setting in MR5. For x8 device, the function of DM is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifing whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH.
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. For x4/x8 based SDRAMs, BG0 and BG1 are valid. For x16 based SDRAM components only BG0 is valid.
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A16	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	CMOS Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific datasheets to determine which DQ is used.
DQS_t, DQS_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR4 SDRAMs support differential data strobe only and does not support single-ended.

Ex. 6 at 7 (datasheet for M386A8K40BM1-CRC).

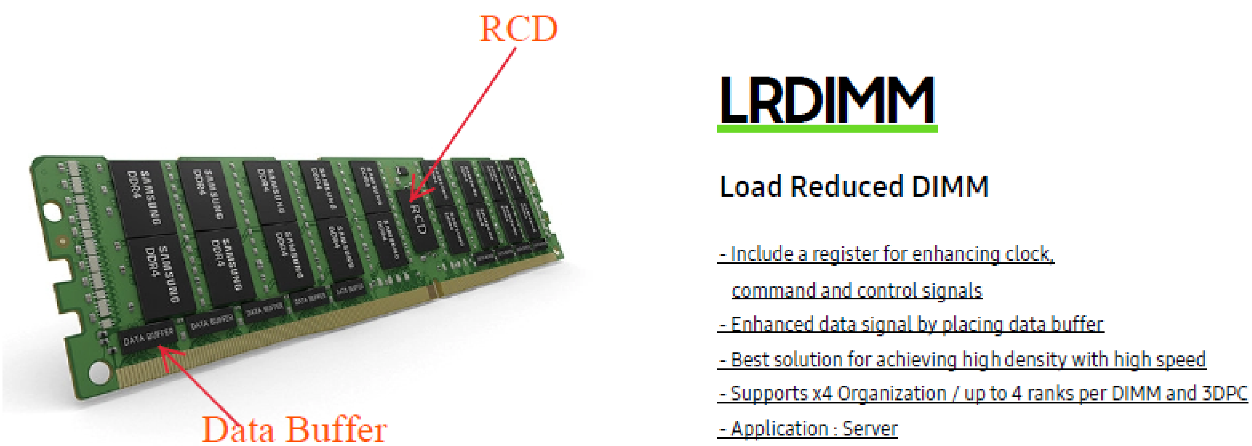


Id. at 10 (datasheet for M386A8K40BM1-CRC).

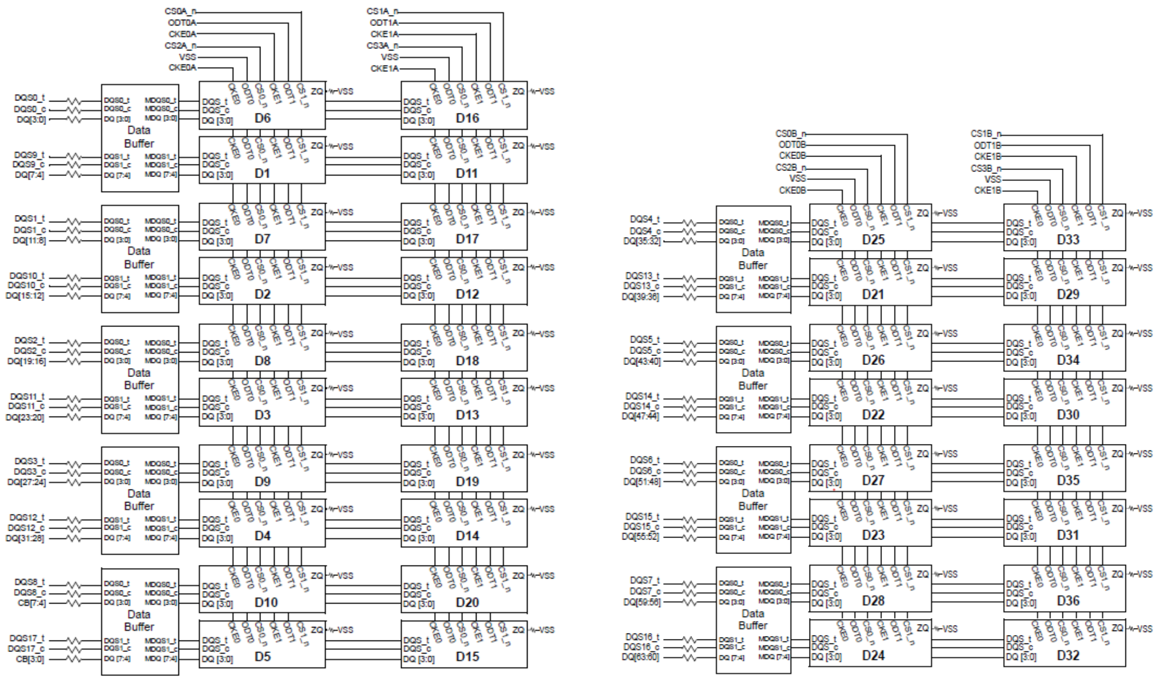


Id. at 11-12. The JEDEC Standard No. 82-32A further discloses the module clock signals as BCK_t/BCK_c. *See* Ex. 7 at 2 (JEDEC Standard No. 82-32A (August 2019)) ("The clock inputs BCK_t and BCK_c are used to sample the control inputs BCOM[3:0], BCKE and BODT. The BCOM[3:0] inputs are used to write device internal control registers.").

74. Each of the accused DDR4 LRDIMMs includes memory devices mounted on the module board and configured to receive the module command signals and the module clock signal, and to perform the memory operations in response to the module command signals. The memory devices include a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines. For example, the accused DDR4 LRDIMM includes:

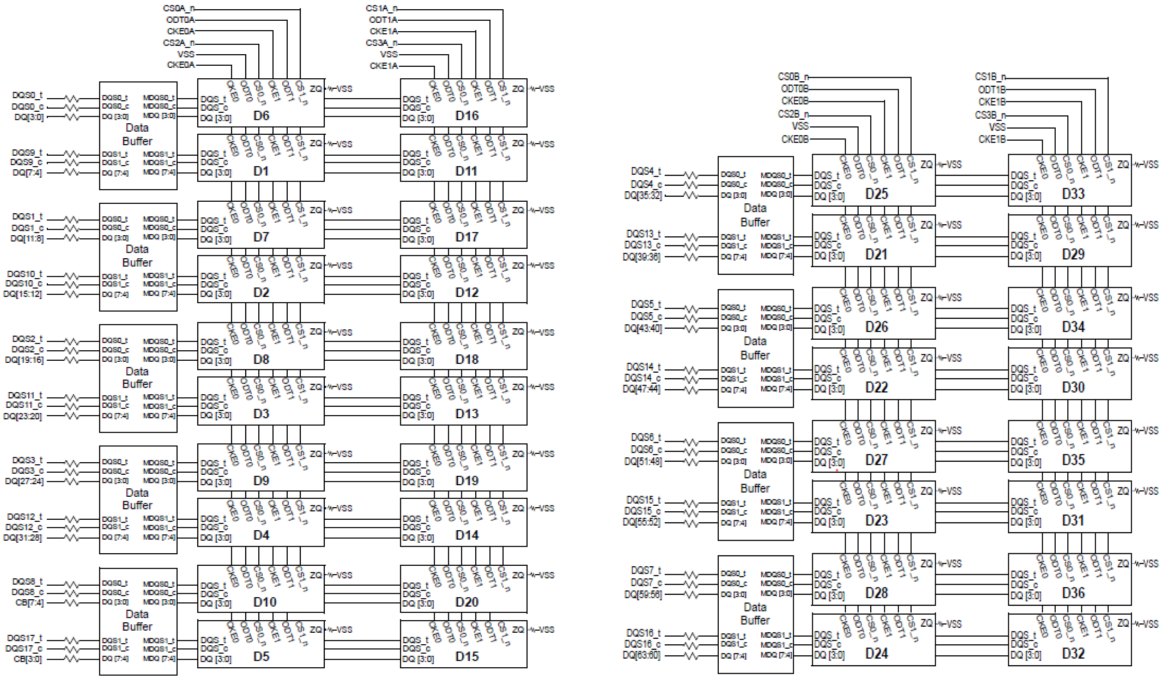


(Annotated depiction of an exemplary Samsung DDR4 LRDIMM advertised on its website, *available at* https://semiconductor.samsung.com/dram/module/lrdimm/m386a8k40bm1-crc/ (last accessed August 13, 2022)).



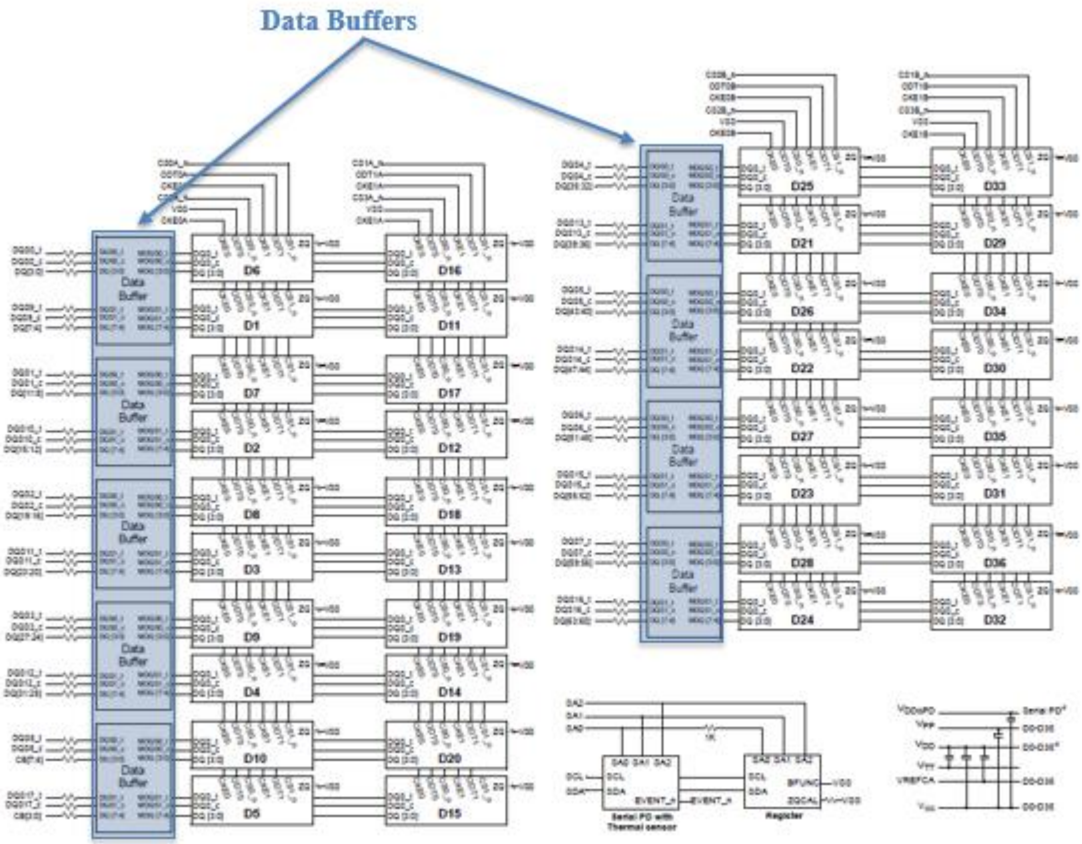
Ex. 6 at 11-12 (datasheet for M386A8K40BM1-CRC).

75. Each of the accused DDR4 LRDIMMs includes a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and a respective set of memory devices, and configured to receive the module control signals and the module clock signal. For example:

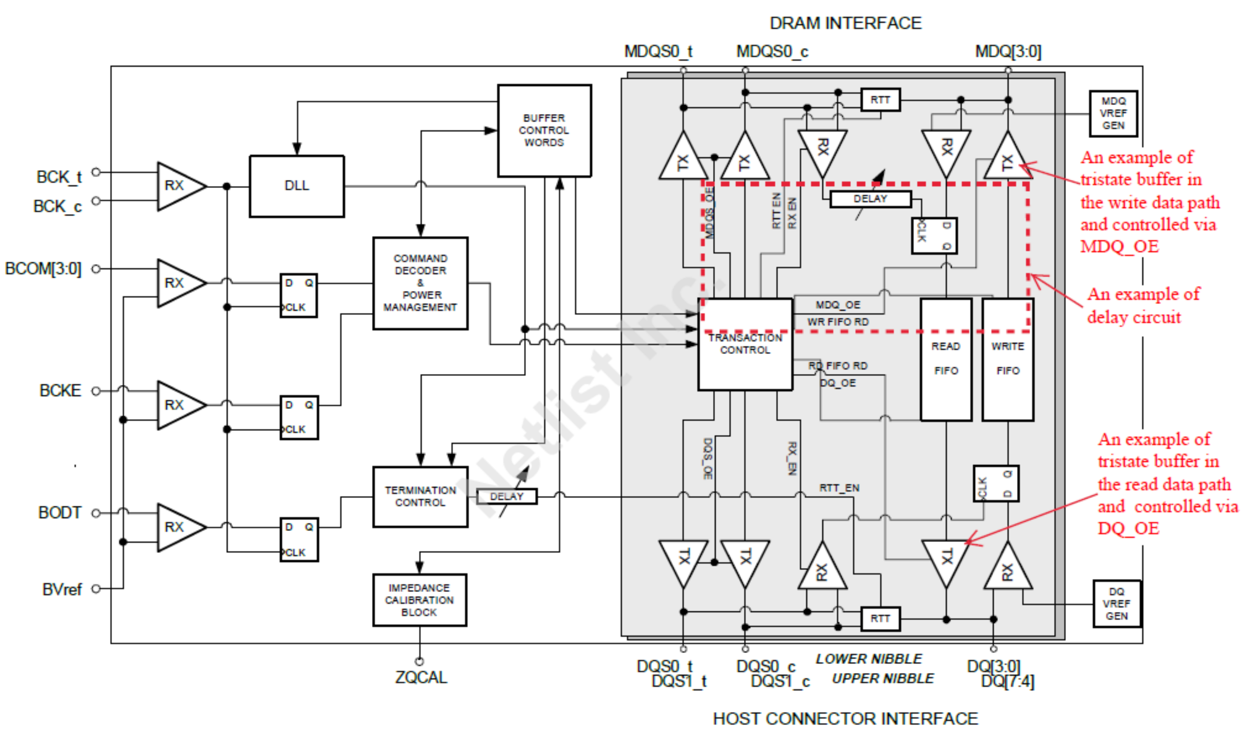


Id. at 11-12 (datasheet for M386A8K40BM1-CRC).

76. Each respective buffer circuit in the accused DDR4 LRDIMMs includes a data path corresponding to each data signal line in the respective set of data/strobe signal lines. Further, each respective buffer circuit in the accused DDR4 LRDIMMs includes a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock signal. For example:

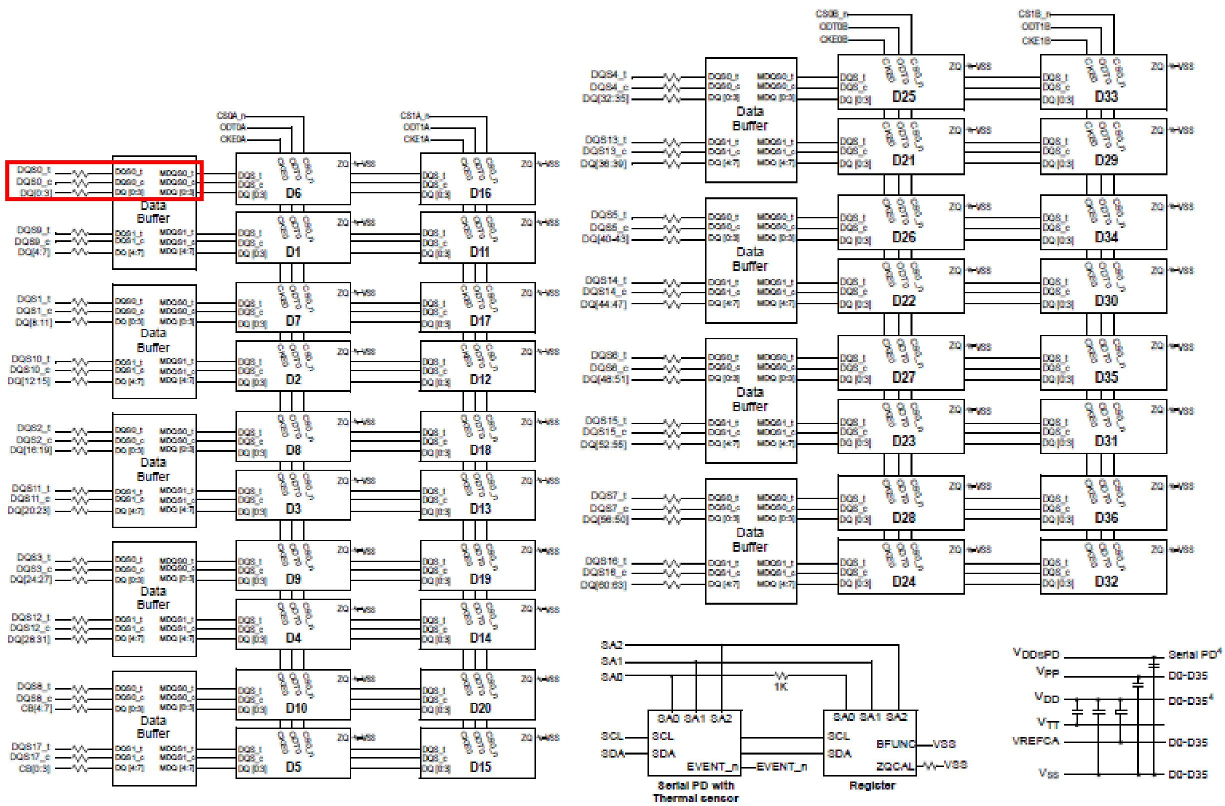


Id. at 11-12 (datasheet for M386A8K40BM1-CRC).



Ex. 7 (JEDEC Standard No. 82-32A (August 2019), Page 95).

77. As shown above in the example block diagram of Fig. 15 at page 95 of JEDEC Standard No. 82-32A, the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit. As shown above and below, the data path corresponding to the each data signal line also includes a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.



Ex. 6 (Datasheet for M386A8K40BM1-CRC) at 11-12.

78. Timing delays to be applied to data and data strobe signals are determined as described in at least section 2.12 starting at page 12 and in Table 16 at page 27 of JEDEC Standard No. 82-32A.

2.12 Command Sequence Descriptions

To accommodate the worst case DRAM CAS Latency, Additive Latency and Parity Latency, a DB is required to support a queue depth of 12 commands on the BCOM bus for data rates up to 2400MT/s.

The timing diagrams in this section show only the lower nibble of the DDR4DB02. The same timing relationships apply independently also for the upper nibble. The timing diagrams only show the case of burst length = 8 and preamble = 1 nCK but equivalent timing relationships exist for burst length = 4 & 10 and preamble = 2 nCK.

For readability reasons, the timing diagrams use the abbreviations DB_RL and DB_WL for the latency between first cycle of RD command and the first rising edge of MDQS at DDR4DB02 inputs and for the latency between first cycle of WR command and the first rising edge of MDQS at DDR4DB02 outputs respectively. Both DB_RL and DB_WL include full cycle and fractional cycle delays. The equations for these latencies are as follows:

DB_WL(R)[1] = CWL + AL + PL + DWL(R)

DB_RL(R)[2] = CL + AL + PL + MRE(R) + tRPRE/2

The equations for DWL and MRE for Ranks 0 to 3 are listed below.

where xxx[R].l and xxx[R].u are the equations for the lower and upper nibbles respectively

DWL[0].l = (F0BCDx[2:0] * 64 + F0BCAx[5:0]) * tCK/64

DWL[0].u = (F0BCDx[6:4] * 64 + F0BCBx[5:0]) * tCK/64

DWL[1].l = (F1BCDx[2:0] * 64 + F1BCAx[5:0]) * tCK/64

DWL[1].u = (F1BCDx[6:4] * 64 + F1BCBx[5:0]) * tCK/64

DWL[2].l = (F0BCFx[2:0] * 64 + F2BCAx[5:0]) * tCK/64

DWL[2].u = (F0BCFx[6:4] * 64 + F2BCBx[5:0]) * tCK/64

DWL[3].l = (F1BCFx[2:0] * 64 + F3BCAx[5:0]) * tCK/64

DWL[3].u = (F1BCFx[6:4] * 64 + F3BCBx[5:0]) * tCK/64

MRE[0].l = (F0BCCx[2:0] * 64 + F0BC2x[5:0]) * tCK/64

MRE[0].u = (F0BCCx[6:4] * 64 + F0BC3x[5:0]) * tCK/64

MRE[1].l = (F1BCCx[2:0] * 64 + F1BC2x[5:0]) * tCK/64

MRE[1].u = (F1BCCx[6:4] * 64 + F1BC3x[5:0]) * tCK/64

MRE[2].l = (F0BCEx[2:0] * 64 + F2BC2x[5:0]) * tCK/64

1.This equation assumes that the DDR4DB02 MDQ-MDQS Write Delay Control Words in F[3:0]BC8x/ F[3:0]BC9x are at their default power-on setting.

2.This equation assumes that the DDR4DB02 MDQS Read Delay Control Words in F[3:0]BC4x/F[3:0]BC5x are at their default power-on setting.

MRE[2].u = (F0BCEx[6:4] * 64 + F2BC3x[5:0]) * tCK/64

MRE[2].l = (F1BCEx[2:0] * 64 + F3BC2x[5:0]) * tCK/64

MRE[2].u = (F1BCEx[6:4] * 64 + F3BC3x[5:0]) * tCK/64

tRPRE/2 exists in DB_RL since the host will adjust the receive enable delay MRE(R) to place it in the center of the read preamble.

The DDR4DB02 delays tPDM_RD and tPDM_WR are defined as the delay between first rising edge of MDQS and the first rising edge of DQS for a RD command and as the delay between first rising edge of DQS and the first rising edge of MDQS for a WR command respectively. By default these delays are constant per DDR4DB02 for all ranks and nibbles.

See Ex. 7] at 11-12 (JEDEC Standard No. 82-32A (August 2019)). Each buffer circuit determines the rank ID of the specific set of memory devices, to be read from or to be written into, by decoding the module control signals, BCOM[3:0], during the second clock cycle after a properly received and decoded read or write commands during the first clock cycle.

Table 4 — Multicycle Sequence for Write Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	WR	Write command BCOM[3:0] = 1000
2	DAT0	Transfer the rank ID for write command BCOM[1:0] = {RANK_ID[1:0]} for DRAM writes Burst length information for Write data BCOM[3:2] = {0, 0} for BC4 BCOM[3:2] = {0, 1} for BC8
3	PAR[3:0]	Even parity bits for WR command and data PAR[x]: Parity bit for previous two BCOM[x] transfers
4	Next Cmd	Next Command

See Id. at 12 (JEDEC Standard No. 82-32A (August 2019)).

Table 5 — Multi-cycle Sequence for Read Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	RD	Read command BCOM[3:0] = 1001
2	DAT0	Transfer the rank ID for read command or the MPR selection ID in MPR override read mode BCOM[1:0] = {RANK_ID[1:0]} for DRAM reads BCOM[1:0] = {BA1, BA0} for MPR override reads Burst length information for Read data BCOM[3:0] = {0, 0} for BC4[1] BCOM[3:0] = {0, 1} for BC8
3	PAR[3:0]	Even parity bits for RD command and data PAR[x]: Parity bit for previous two BCOM[x] transfers
4	Next Cmd	Next Command

*See Id.*at 14 (JEDEC Standard No. 82-32A, (August 2019)).

Table 16 — Timing and Training Control Words

Address	Description	Scope
BC0C	Training control word	Training mode enable
F0BCCx	Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable Control Word for Rank 0	Additional cycles of DRAM Interface Receive Enable Delay and Write Leveling Delay per rank and per nibble
F0BCDx	Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling Control Word for Rank 0	
F0BCEx	Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable Control Word for Rank 2	
F0BCFx	Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling Control Word for Rank 2	
F1BCCx	Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable Control Word for Rank 1	
F1BCDx	Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling Control Word for Rank 1	
F1BCEx	Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable Control Word for Rank 3	
F1BCFx	Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling Control Word for Rank 3	
F[3:0]BC2x	Lower nibble DRAM interface receive enable training control	DRAM Interface Receive Enable phase and cycle control per rank
F[3:0]BC3x	Upper nibble DRAM interface receive enable training control	
F[3:0]BC4x	Lower nibble MDQS read delay control	Input MDQS delay control per rank
F[3:0]BC5x	Upper nibble MDQS read delay control	
F[3:0]BC8x	Lower nibble MDQ-MDQS write delay control	Output MDQ signal phase control per rank
F[3:0]BC9x	Upper nibble MDQ-MDQS write delay control	
F[3:0]BCAx	Lower nibble host interface write leveling control	Host Interface write leveling phase and cycle control per rank
F[3:0]BCBx	Upper nibble host interface write leveling training control	
F5BC0x - F5BC3x F6BC0x - F6BC3x	Lower and upper nibble Multi Purpose Registers[7:0]	Store read/write data patterns for receive enable, read and write delay and host interface write training as well as MPR override mode.
F6BC4x	Buffer training configuration control word	Configuration control for certain training modes
F6BC5x	Buffer training status word	Status for certain training modes
F[7:4]BC8x	MDQ0/4-Read delay control	Input MDQS delay control per rank and per lane
F[7:4]BC9x	MDQ1/5-Read delay control	
F[7:4]BCAx	MDQ2/6-Read delay control	
F[7:4]BCBx	MDQ3/7-Read delay control	
F[7:4]BCCx	MDQ0/4-MDQS write delay control	Output MDQ signal phase control per rank and per lane
F[7:4]BCDx	MDQ1/5-MDQS write delay control	
F[7:4]BCEx	MDQ2/6-MDQS write delay control	
F[7:4]BCFx	MDQ3/7-MDQS write delay control	

See Id. at 27 (JEDEC Standard No. 82-32A (August 2019)) (demonstrating timing control registers and fields corresponding to timing delays information per rank and/or per lower or upper nibble of each buffer circuit).

79. On information and belief, Samsung also indirectly infringes the ’608 patent, as provided in 35 U.S.C. § 271(b), by inducing infringement by others, such as Samsung’s customers and end users, in this District and elsewhere in the United States. For example, on information

and belief, Samsung has induced, and currently induces, the infringement of the ’608 patent through its affirmative acts of selling, offering to sell, distributing, and/or otherwise making available the accused DDR4 LRDIMM products and other materially similar products that infringe the ’608 patent. On information and belief, Samsung provides, and has provided, specifications, datasheets, instruction manuals, and/or other materials that encourage and facilitate infringing use of the accused DDR4 LRDIMM products and other materially similar products by users in a manner that it knows or should have known would result in infringement and with the intent of inducing infringement.

80. On information and belief, Samsung also indirectly infringes the ’608 patent, as provided in 35 U.S.C. § 271(c), by contributing to direct infringement committed by others, such as customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Samsung has contributed to, and currently contributes to, Samsung’s customers’ and end-users’ infringement of the ’608 patent through its affirmative acts of selling and offering to sell, in this District and elsewhere in the United States, the accused DDR4 LRDIMM products and other materially similar products that infringe the ’608 patent. On information and belief, the accused DDR4 LRDIMM and other materially similar products have no substantial noninfringing use, and constitute a material part of the patented invention. On information and belief, Samsung is aware that the product or process that includes the accused DDR4 LRDIMM products and other materially similar products would be covered by one or more claims of the ’608 patent. On information and belief, the use of the product or process that includes the accused DDR4 LRDIMM products infringes at least one claim of the ’608 patent.

81. Samsung’s infringement of the ’608 patent has damaged and will continue to damage Netlist. Samsung has had knowledge of Netlist’s technology since as early as 2010. Samsung has had knowledge of U.S. Pat. Application Nos. 13/952,599 and/or 14/846,993, to

which the ’608 patent claims priority, as early as 2016, when Netlist provided Samsung with a list of its patents including predecessor patents to the ’608. Samsung gained knowledge of the ’608 patent no later than August 2, 2021, when Netlist provided Samsung with a list of Netlist patents, including the ’608 patent. Samsung’s infringement of the ’608 patent has been continuous and willful. Samsung continues to commit acts of infringement despite a high likelihood that its actions constitute infringement, and Samsung knew or should have known that its actions constituted an unjustifiably high risk of infringement.

VIII. DEMAND FOR JURY TRIAL

82. Pursuant to Federal Rule of Civil Procedure 38(b), Netlist hereby demands a trial by jury on all issues triable to a jury.

IX. PRAYER FOR RELIEF

WHEREFORE, Netlist respectfully requests that this Court enter judgment in its favor ordering, finding, declaring, and/or awarding Netlist relief as follows:

A. that Samsung directly and/or indirectly infringes the Patents-in-Suit;

B. all equitable relief the Court deems just and proper as a result of Samsung’s infringement;

C. an award of damages resulting from Samsung’s acts of infringement in accordance with 35 U.S.C. § 284;

D. that Samsung’s infringement of each of the Patents-in-Suit is willful;

E. enhanced damages pursuant to 35 U.S.C. § 284;

F. that this is an exceptional case and awarding Netlist its reasonable attorneys’ fees pursuant to 35 U.S.C. § 285;

G. an accounting for acts of infringement and supplemental damages, without limitation, prejudgment and post-judgment interest; and